

ABSTRACT

A shallow-trench isolation transistor includes an active region in a semiconductor substrate bounded by an isolation trench. The active region in the semiconductor substrate includes spaced apart source and drain regions and a gate 5 lies above, between, and insulated from the source and drain regions. A sidewall channel-stop implant is formed in the side and bottom walls of the isolation trench and extends below the level of the source and drain implants in the active transistor region and significantly lowers the radiation-induced leakage currents that would otherwise exist in the shallow-trench isolation transistor. A 10 method for fabricating a shallow-trench isolation transistor includes forming isolation trenches to define active regions in a silicon substrate; performing sidewall isolation implants on the side and bottom walls of the isolation trenches; depositing a dielectric isolation material in the isolation trenches; planarizing the top surface of the silicon substrate and the dielectric isolation material; forming a 15 gate oxide layer over the active regions in the silicon substrate; forming and defining gate regions over the gate oxide layer in the active regions in the silicon substrate; and forming source and drain regions in the active regions in the silicon substrate.